Amendment history of SSD1309 Specification

Revision	Description of any change	Issued	Effective
0.10 C7KA3 07-Oct-10	Reference from SPD0301 Rev1.0 with following changes: 1. Rename GPIO pin into TR7, LS pin into V_{SS1} (Block Diagram, Pad coordinate, Pin description and application example) 2. Round off die size to 1 d.p. 3. Re-arrange command table sequence according to function 4. Remove note 2 in command 21h 5. Remove note 1 in command A0/A1h 6. Revise command 22h fromA[3:0] to A[2:0], from B[3:0] to B[2:0] 7. Remove Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh 8. Remove command description for "Status register Read" 9. Add Content Scrolling software flow example in command description of 2Ch/2Dh Approver list: Product Marketing- Raymond Ho Design Engineering-Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing- Daniel Ho TE / TPE - Warren Wong	Janette Wong	12-Oct-10
1.0 C7KA3 13-Oct-10	1. Change to Adv info 2. Remove confidential watermark 3. Add SSD1309UR1 in ordering information (P.11 , P.55) Approver list: Product Marketing- Raymond Ho Design Engineering-Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing- Daniel Ho TE / TPE - Warren Wong / Stephen Leung	Ada Ng	14-Oct-10
1.1 C7KA3 19-Jul-11	1. Added Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh in Section 9 & Section 10 2. Revised default value of A[7:4] of command D5h in Table 9-5 from 1000b into 0111b. (P.34) Approver list: Product Marketing- Ringo Lau Design Engineering-Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing- Daniel Ho TE / TPE - Warren Wong / Stephen Leung	Janette Wong	27-Jul-11

SSD1309

Advance Information

128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1309 Specification

Version	Change Items	Effective Date
0.10	1st Release	12-Oct-10
1.0	1. Changed to Advance Information 2. Add SSD1309UR1 in ordering information. (P.11 , P.55)	14-Oct-10
1.1	1. Added Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh in Section 9 & Section 10 (P.28~31, P.33, P.45~48) 2. Revised default value of A[7:4] of command D5h in Table 9-5 from 1000b into 0111b. (P.34)	27-Jul-11

CONTENT

FIGURES

TABLE

1 GENERAL DESCRIPTION

SSD1309 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1309 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V_{DD} = 1.65V ~ 3.3V for IC logic
  - V_{CC} = 7.0V ~ 16.0V for Panel driving
- For matrix display
  - OLED driving output voltage, 16V maximum
  - Segment maximum source current: 320uA
  - Common maximum sink current: 40mA
  - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving infinite content scrolling function
- Programmable Frame Rate
- Programmable Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

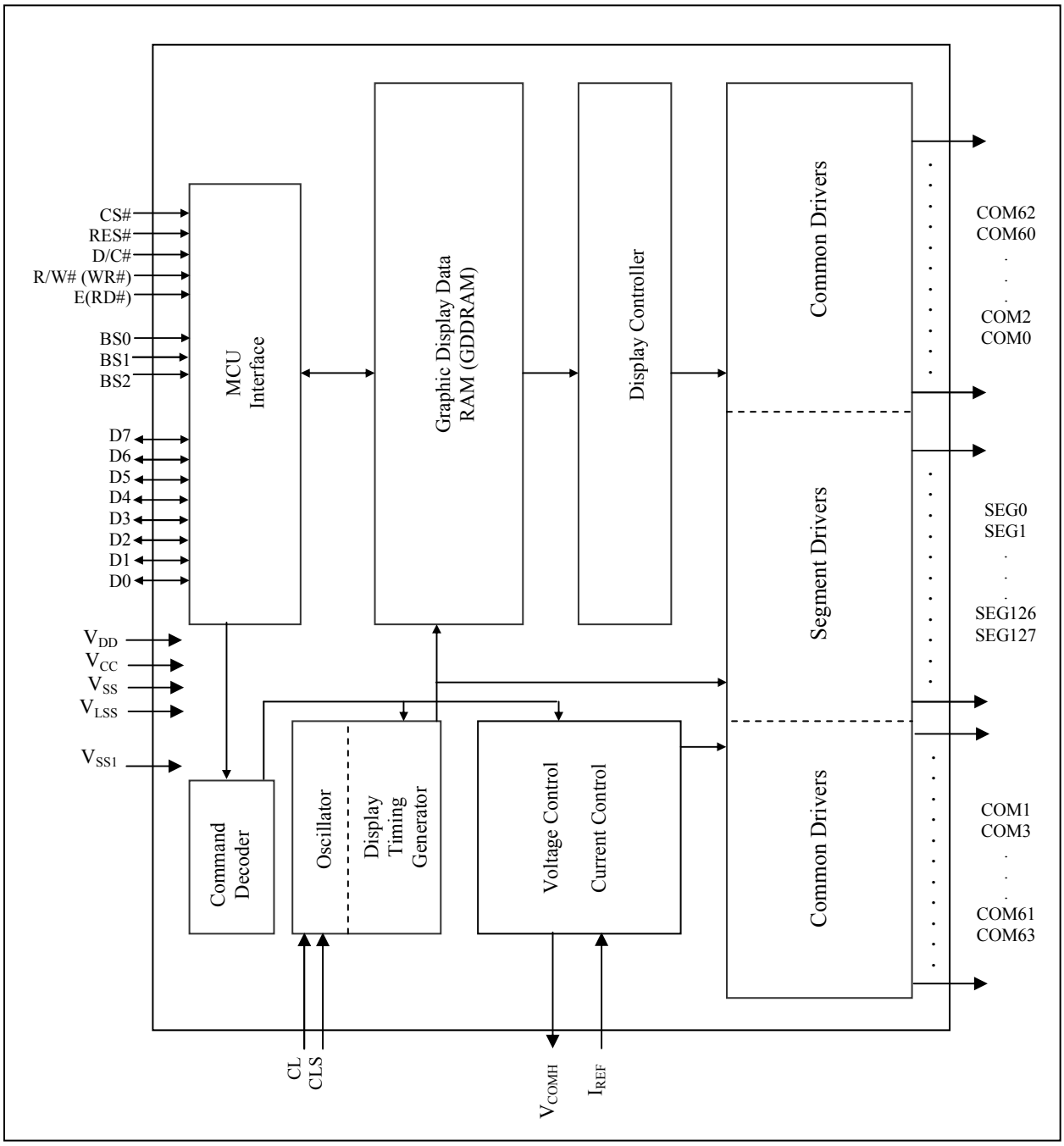
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1309Z	128	64	COG	Page 9	o Min SEG pad pitch : 37.5um o Min COM pad pitch : 27um o Min I/O pad pitch : 60 um o Die thickness : 300 +/- 15 um
SSD1309UR1	128	64	COF	Page 11,61	o35mm film, 4 sprocket hole oHot bar type COF o8-bit 80 / 8-bit 68 / SPI / I2C interface oSEG lead pitch 0.120mm x 0.998 =0.11976mm oCOM lead pitch 0.120mm x 0.998 =0.11976mm

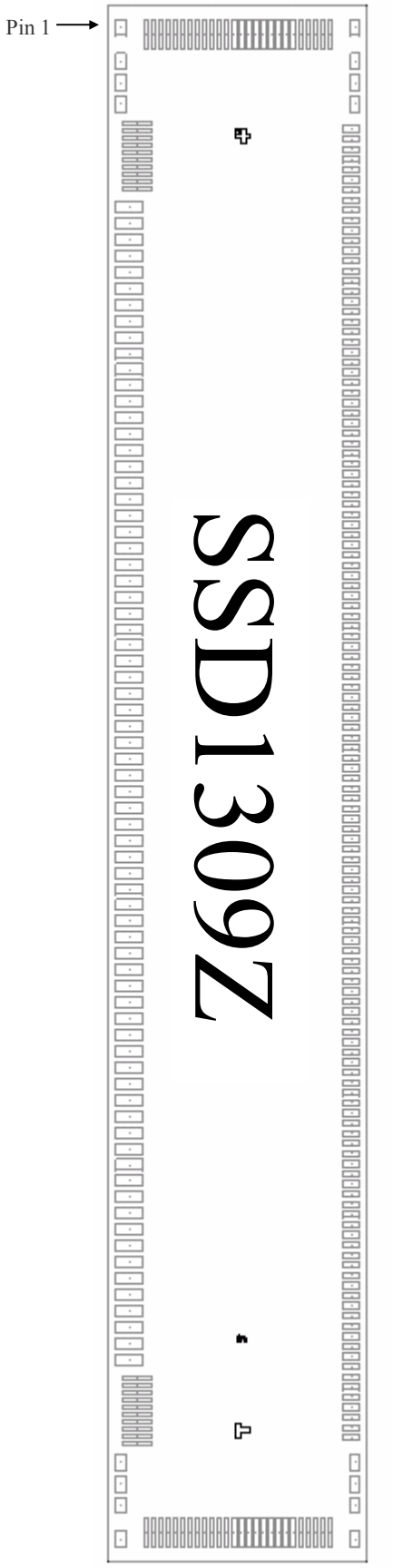
4 BLOCK DIAGRAM

Figure 4-1 : SSD1309 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1309Z Die Drawing



Die size (after sawing)	5.8 ± 0.05mm x 1.0 ± 0.05mm
Die thickness	300 +/- 15um
Min I/O pad pitch	60um
Min SEG pad pitch	37.5um
Min COM pad pitch	27um
Bump height	Nominal 12um

Bump size		
Pad#	X[um]	Y[um]
1~4, 97~100, 127~130, 261~264	59	35
5~14, 87~96	15	108
101~126, 265~290	108	15
15~86	40	100
131~260	22	64

Alignment mark	Position	Size
+ shape	(-2392.2, 18.8)	56.25um x 56.25um
T shape	(2392.2, 18.8)	56.25um x 56.25um
SSL Logo	(2055, 20)	-

(For details dimension please see Figure 5-2)

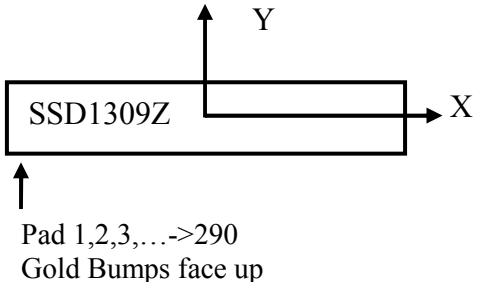


Figure 5-2: SSD1309Z alignment mark dimension

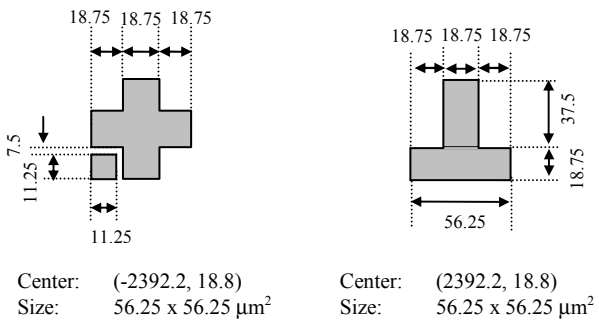


Table 5-1: SSD1309Z Bump Die Pad Coordinates

Pin number	Pin name	X	Y
1	VCOMH	-2794.52	-431.5
2	VCOMH	-2668.32	-431.5
3	VCOMH	-2589.32	-431.5
4	VCOMH	-2510.32	-431.5
5	VLSS	-2439.76	-371.02
6	COM56	-2412.76	-371.02
7	COM57	-2385.76	-371.02
8	COM58	-2358.76	-371.02
9	COM59	-2331.76	-371.02
10	COM60	-2304.76	-371.02
11	COM61	-2277.76	-371.02
12	COM62	-2250.76	-371.02
13	COM63	-2223.76	-371.02
14	VCOMH	-2196.76	-371.02
15	NC	-2130	-399
16	VLSS	-2070	-399
17	VLSS	-2010	-399
18	VLSS	-1950	-399
19	NC	-1890	-399
20	VCC	-1830	-399
21	VCC	-1770	-399
22	VCC	-1710	-399
23	VCC	-1650	-399
24	VCOMH	-1590	-399
25	VCOMH	-1530	-399
26	VCOMH	-1470	-399
27	VCOMH	-1410	-399
28	NC	-1350	-399
29	VSS	-1290	-399
30	VSS	-1230	-399
31	VSS	-1170	-399
32	VDD	-1110	-399
33	VDD	-1050	-399
34	VDD	-990	-399
35	BS0	-930	-399
36	VSS	-870	-399
37	BS1	-810	-399
38	VDD	-750	-399
39	BS2	-690	-399
40	VSS	-630	-399
41	TR7	-570	-399
42	VSS1	-510	-399
43	CL	-450	-399
44	VSS	-390	-399
45	CS#	-330	-399
46	RES#	-270	-399
47	D/C#	-210	-399
48	VSS	-150	-399
49	R/W#(WR#)	-90	-399
50	E(RD#)	-30	-399
51	D0	30	-399
52	D1	90	-399
53	D2	150	-399
54	D3	210	-399
55	VSS	270	-399
56	D4	330	-399
57	D5	390	-399
58	D6	450	-399
59	D7	510	-399
60	IREF	570	-399
61	VSS	630	-399
62	CLS	690	-399
63	VDD	750	-399
64	VDD	810	-399
65	VCOMH	870	-399
66	VCOMH	930	-399
67	VCOMH	990	-399
68	VCOMH	1050	-399
69	VCC	1110	-399
70	VCC	1170	-399
71	VCC	1230	-399
72	VCC	1290	-399
73	VCC	1350	-399
74	NC	1410	-399
75	VLSS	1470	-399
76	VLSS	1530	-399
77	VLSS	1590	-399
78	TR6	1650	-399
79	TR5	1710	-399
80	TR4	1770	-399

Pin number	Pin name	X	Y
81	VSS	1830	-399
82	TR3	1890	-399
83	TR2	1950	-399
84	TR1	2010	-399
85	TR0	2070	-399
86	VCC	2130	-399
87	VCOMH	2196.76	-371.02
88	COM31	2223.76	-371.02
89	COM30	2250.76	-371.02
90	COM29	2277.76	-371.02
91	COM28	2304.76	-371.02
92	COM27	2331.76	-371.02
93	COM26	2358.76	-371.02
94	COM25	2385.76	-371.02
95	COM24	2412.76	-371.02
96	VLSS	2439.76	-371.02
97	VCOMH	2510.32	-431.5
98	VCOMH	2589.32	-431.5
99	VCOMH	2668.32	-431.5
100	VCOMH	2794.52	-431.5
101	VCOMH	2770.02	-337.5
102	COM23	2770.02	-310.5
103	COM22	2770.02	-283.5
104	COM21	2770.02	-256.5
105	COM20	2770.02	-229.5
106	COM19	2770.02	-202.5
107	COM18	2770.02	-175.5
108	COM17	2770.02	-148.5
109	COM16	2770.02	-121.5
110	COM15	2770.02	-94.5
111	COM14	2770.02	-67.5
112	COM13	2770.02	-40.5
113	COM12	2770.02	-13.5
114	COM11	2770.02	13.5
115	COM10	2770.02	40.5
116	COM9	2770.02	67.5
117	COM8	2770.02	94.5
118	COM7	2770.02	121.5
119	COM6	2770.02	148.5
120	COM5	2770.02	175.5
121	COM4	2770.02	202.5
122	COM3	2770.02	229.5
123	COM2	2770.02	256.5
124	COM1	2770.02	283.5
125	COM0	2770.02	310.5
126	VSS	2770.02	337.5
127	VCOMH	2794.52	431.5
128	VCC	2668.32	431.5
129	VCC	2589.32	431.5
130	VCC	2510.32	431.5
131	VCC	2418.75	417
132	SEG0	2381.25	417
133	SEG1	2343.75	417
134	SEG2	2306.25	417
135	SEG3	2268.75	417
136	SEG4	2231.25	417
137	SEG5	2193.75	417
138	SEG6	2156.25	417
139	SEG7	2118.75	417
140	SEG8	2081.25	417
141	SEG9	2043.75	417
142	SEG10	2006.25	417
143	SEG11	1968.75	417
144	SEG12	1931.25	417
145	SEG13	1893.75	417
146	SEG14	1856.25	417
147	SEG15	1818.75	417
148	SEG16	1781.25	417
149	SEG17	1743.75	417
150	SEG18	1706.25	417
151	SEG19	1668.75	417
152	SEG20	1631.25	417
153	SEG21	1593.75	417
154	SEG22	1556.25	417
155	SEG23	1518.75	417
156	SEG24	1481.25	417
157	SEG25	1443.75	417
158	SEG26	1406.25	417
159	SEG27	1368.75	417
160	SEG28	1331.25	417

Pin number	Pin name	X	Y
161	SEG29	1293.75	417
162	SEG30	1256.25	417
163	SEG31	1218.75	417
164	SEG32	1181.25	417
165	SEG33	1143.75	417
166	SEG34	1106.25	417
167	SEG35	1068.75	417
168	SEG36	1031.25	417
169	SEG37	993.75	417
170	SEG38	956.25	417
171	SEG39	918.75	417
172	SEG40	881.25	417
173	SEG41	843.75	417
174	SEG42	806.25	417
175	SEG43	768.75	417
176	SEG44	731.25	417
177	SEG45	693.75	417
178	SEG46	656.25	417
179	SEG47	618.75	417
180	SEG48	581.25	417
181	SEG49	543.75	417
182	SEG50	506.25	417
183	SEG51	468.75	417
184	SEG52	431.25	417
185	SEG53	393.75	417
186	SEG54	356.25	417
187	SEG55	318.75	417
188	SEG56	281.25	417
189	SEG57	243.75	417
190	SEG58	206.25	417
191	SEG59	168.75	417
192	SEG60	131.25	417
193	SEG61	93.75	417
194	SEG62	56.25	417
195	SEG63	18.75	417
196	SEG64	-18.75	417
197	SEG65	-56.25	417
198	SEG66	-93.75	417
199	SEG67	-131.25	417
200	SEG68	-168.75	417
201	SEG69	-206.25	417
202	SEG70	-243.75	417
203	SEG71	-281.25	417
204	SEG72	-318.75	417
205	SEG73	-356.25	417
206	SEG74	-393.75	417
207	SEG75	-431.25	417
208	SEG76	-468.75	417
209	SEG77	-506.25	417
210	SEG78	-543.75	417
211	SEG79	-581.25	417
212	SEG80	-618.75	417
213	SEG81	-656.25	417
214	SEG82	-693.75	417
215	SEG83	-731.25	417
216	SEG84	-768.75	417
217	SEG85	-806.25	417
218	SEG86	-843.75	417
219	SEG87	-881.25	417
220	SEG88	-918.75	417
221	SEG89	-956.25	417
222	SEG90	-993.75	417
223	SEG91	-1031.25	417
224	SEG92	-1068.75	417
225	SEG93	-1106.25	417
226	SEG94	-1143.75	417
227	SEG95	-1181.25	417
228	SEG96	-1218.75	417
229	SEG97	-1256.25	417
230	SEG98	-1293.75	417
231	SEG99	-1331.25	417
232	SEG100	-1368.75	417
233	SEG101	-1406.25	417
234	SEG102	-1443.75	417
235	SEG103	-1481.25	417
236	SEG104	-1518.75	417
237	SEG105	-1556.25	417
238	SEG106	-1593.75	417
239	SEG107	-1631.25	417
240	SEG108	-1668.75	417

Pin number	Pin name	X	Y
241	SEG109	-1706.25	417
242	SEG110	-1743.75	417
243	SEG111	-1781.25	417
244	SEG112	-1818.75	417
245	SEG113	-1856.25	417
246	SEG114	-1893.75	417
247	SEG115	-1931.25	417
248	SEG116	-1968.75	417
249	SEG117	-2006.25	417
250	SEG118	-2043.75	417
251	SEG119	-2081.25	417
252	SEG120	-2118.75	417
253	SEG121	-2156.25	417
254	SEG122	-2193.75	417
255	SEG123	-2231.25	417
256	SEG124	-2268.75	417
257	SEG125	-2306.25	417
258	SEG126	-2343.75	417
259	SEG127	-2381.25	417
260	VCC	-2418.75	417
261	VCC	-2510.32	431.5
262	VCC	-2589.32	431.5
263	VCC	-2668.32	431.5
264	VCOMH	-2794.52	431.5
265	VSS	-2770.02	337.5
266	COM32	-2770.02	310.5
267	COM33	-2770.02	283.5
268	COM34	-2770.02	256.5
269	COM35	-2770.02	229.5
270	COM36	-2770.02	202.5
271	COM37	-2770.02	175.5
272	COM38	-2770.02	148.5
273	COM39	-2770.02	121.5
274	COM40	-2770.02	94.5
275	COM41	-2770.02	67.5
276	COM42	-2770.02	40.5
277	COM43	-2770.02	13.5
278	COM44	-2770.02	-13.5
279	COM45	-2770.02	-40.5
280	COM46	-2770.02	-67.5
281	COM47	-2770.02	-94.5
282	COM48	-2770.02	-121.5
283	COM49	-2770.02	-148.5
284	COM50	-2770.02	-175.5
285	COM51	-2770.02	-202.5
286	COM52	-2770.02	-229.5
287	COM53	-2770.02	-256.5
288	COM54	-2770.02	-283.5
289	COM55	-2770.02	-310.5
290	VCOMH	-2770.02	-337.5

6 PIN ARRANGEMENT

6.1 SSD1309UR1 pin assignment

Figure 6-1 : SSD1309UR1 Pin Assignment

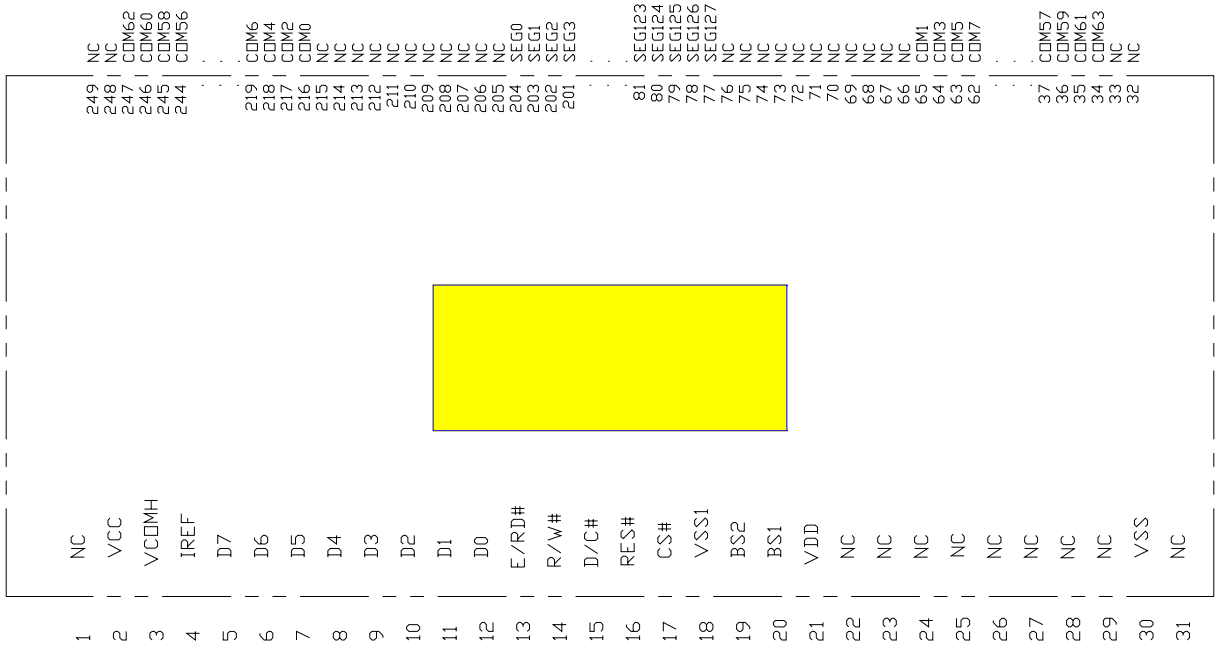


Table 6-1 : SSD1309UR1 Pin Assignment Table

Pin #	Name
1	NC
2	VCC
3	VCOMH
4	IREF
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E(RD#)
14	R/W#
15	D/C#
16	RES#
17	CS#
18	VSS1
19	BS2
20	BS1
21	VDD
22	NC
23	NC
24	NC
25	NC
26	NC
27	NC
28	NC
29	NC
30	VSS
31	NC
32	NC
33	NC
34	COM63
35	COM61
36	COM59
37	COM57
38	COM55
39	COM53
40	COM51
41	COM49
42	COM47
43	COM45
44	COM43
45	COM41
46	COM39
47	COM37
48	COM35
49	COM33
50	COM31
51	COM29
52	COM27
53	COM25
54	COM23
55	COM21
56	COM19
57	COM17
58	COM15
59	COM13
60	COM11
61	COM9
62	COM7
63	COM5
64	COM3
65	COM1
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	NC
75	NC
76	NC
77	SEG127
78	SEG126
79	SEG125
80	SEG124

Pin #	Name
81	SEG123
82	SEG122
83	SEG121
84	SEG120
85	SEG119
86	SEG118
87	SEG117
88	SEG116
89	SEG115
90	SEG114
91	SEG113
92	SEG112
93	SEG111
94	SEG110
95	SEG109
96	SEG108
97	SEG107
98	SEG106
99	SEG105
100	SEG104
101	SEG103
102	SEG102
103	SEG101
104	SEG100
105	SEG99
106	SEG98
107	SEG97
108	SEG96
109	SEG95
110	SEG94
111	SEG93
112	SEG92
113	SEG91
114	SEG90
115	SEG89
116	SEG88
117	SEG87
118	SEG86
119	SEG85
120	SEG84
121	SEG83
122	SEG82
123	SEG81
124	SEG80
125	SEG79
126	SEG78
127	SEG77
128	SEG76
129	SEG75
130	SEG74
131	SEG73
132	SEG72
133	SEG71
134	SEG70
135	SEG69
136	SEG68
137	SEG67
138	SEG66
139	SEG65
140	SEG64
141	SEG63
142	SEG62
143	SEG61
144	SEG60
145	SEG59
146	SEG58
147	SEG57
148	SEG56
149	SEG55
150	SEG54
151	SEG53
152	SEG52
153	SEG51
154	SEG50
155	SEG49
156	SEG48
157	SEG47
158	SEG46
159	SEG45
160	SEG44

Pin #	Name
161	SEG43
162	SEG42
163	SEG41
164	SEG40
165	SEG39
166	SEG38
167	SEG37
168	SEG36
169	SEG35
170	SEG34
171	SEG33
172	SEG32
173	SEG31
174	SEG30
175	SEG29
176	SEG28
177	SEG27
178	SEG26
179	SEG25
180	SEG24
181	SEG23
182	SEG22
183	SEG21
184	SEG20
185	SEG19
186	SEG18
187	SEG17
188	SEG16
189	SEG15
190	SEG14
191	SEG13
192	SEG12
193	SEG11
194	SEG10
195	SEG9
196	SEG8
197	SEG7
198	SEG6
199	SEG5
200	SEG4
201	SEG3
202	SEG2
203	SEG1
204	SEG0
205	NC
206	NC
207	NC
208	NC
209	NC
210	NC
211	NC
212	NC
213	NC
214	NC
215	NC
216	COM0
217	COM2
218	COM4
219	COM6
220	COM8
221	COM10
222	COM12
223	COM14
224	COM16
225	COM18
226	COM20
227	COM22
228	COM24
229	COM26
230	COM28
231	COM30
232	COM32
233	COM34
234	COM36
235	COM38
236	COM40
237	COM42
238	COM44
239	COM46
240	COM48

Pin #	Name
241	COM50
242	COM52
243	COM54
244	COM56
245	COM58
246	COM60
247	COM62
248	NC
249	NC

7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 7-1 : SSD1309 Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
V_{SS1}	-	Reserved Pin. It must be connected to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
BS[2:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. **Table 7-2 : Bus Interface selection** BS[2:0] / Interface 000 / 4 line SPI 001 / 3 line SPI 010 / I^2C 110 / 8-bit 8080 parallel 100 / 8-bit 6800 parallel **Note** (1) 0 is connected to V_{SS} (2) 1 is connected to V_{DD}
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to Figure 8-15 for the details of resistor value
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.

Pin Name	Pin Type	Description
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams Figure 13-1 to Figure 13-5
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
TR[7:0]	-	Reserved pin and is recommended to keep it float.
NC	-	This is dummy pin. Do not group or short NC pins together.

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1309 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-2 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

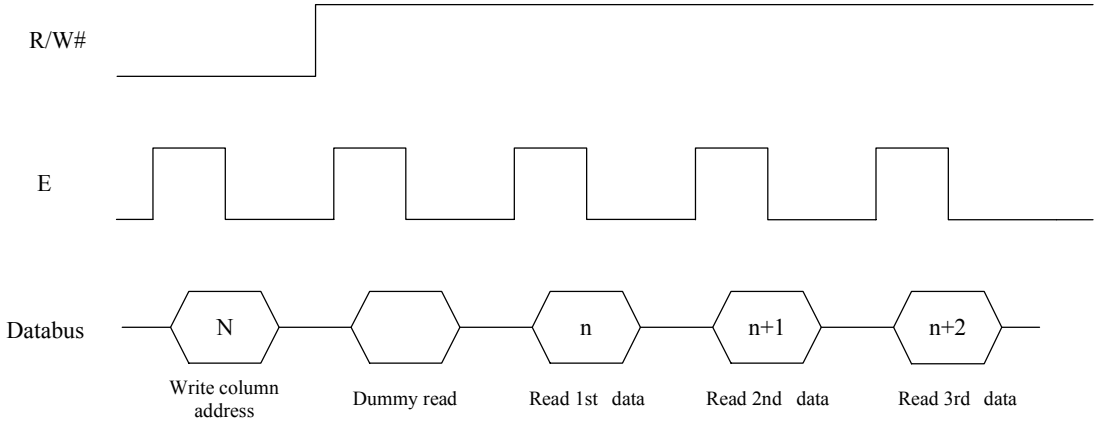
Table 8-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

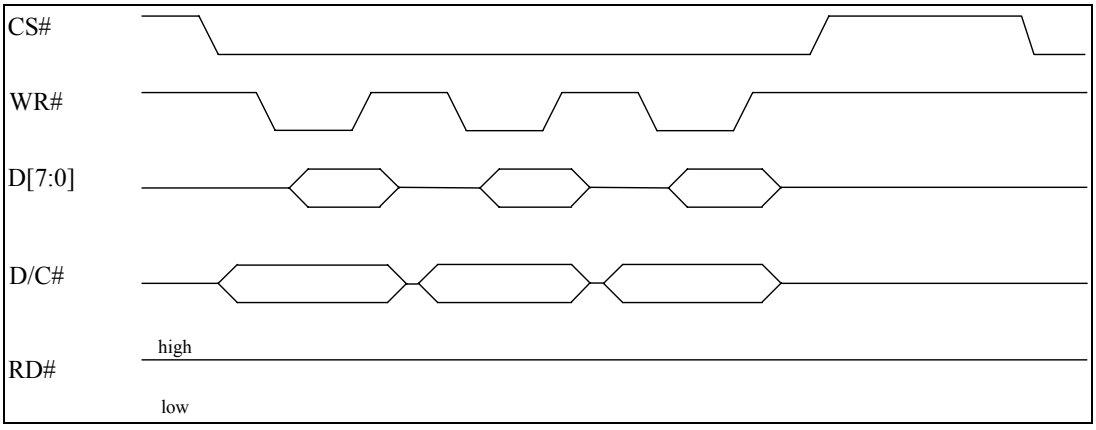


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

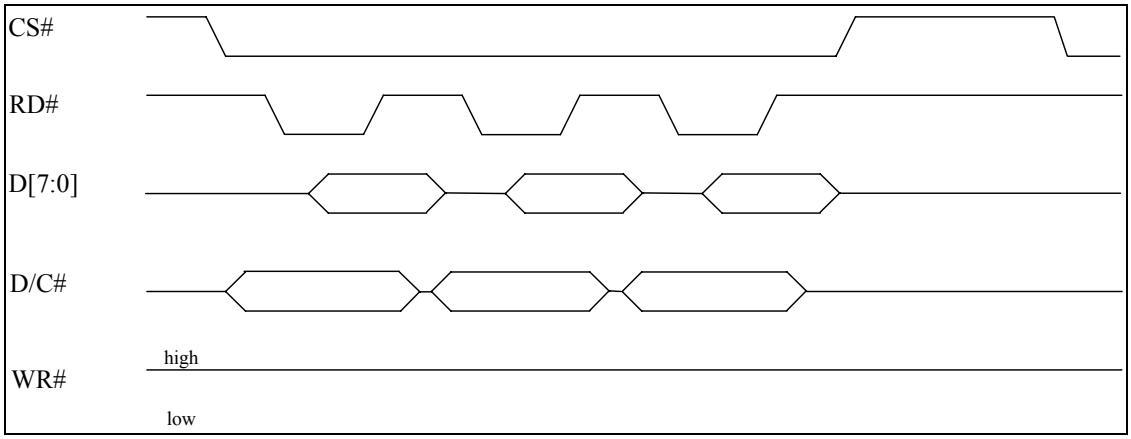


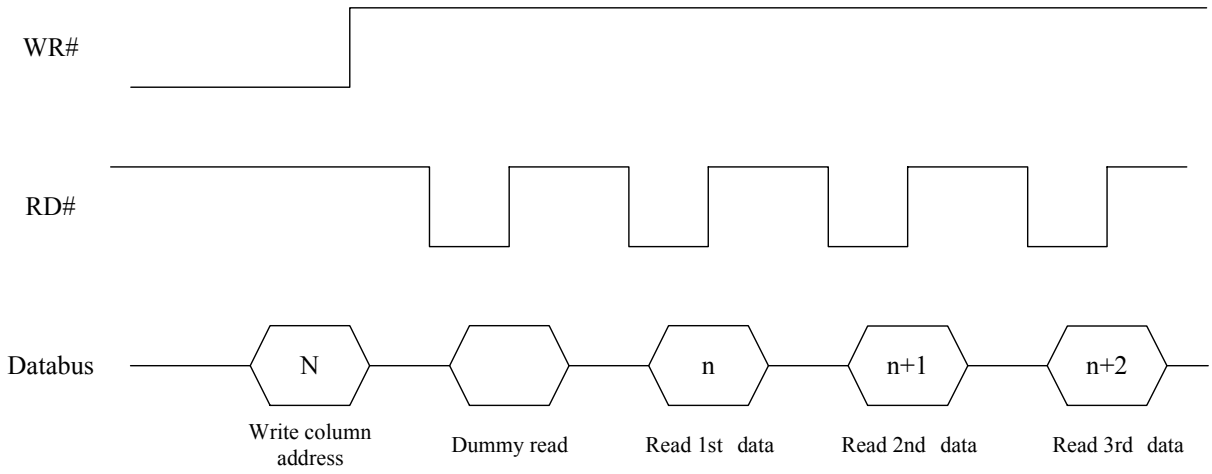
Table 8-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

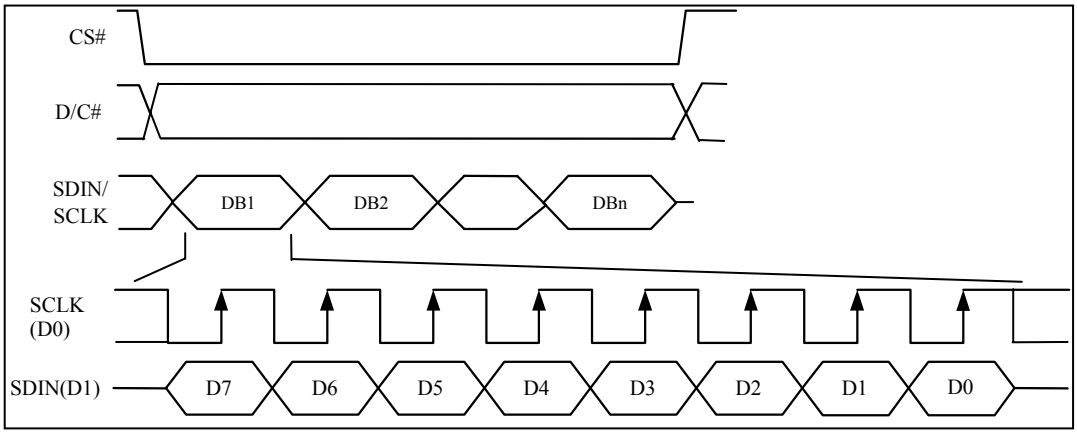
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

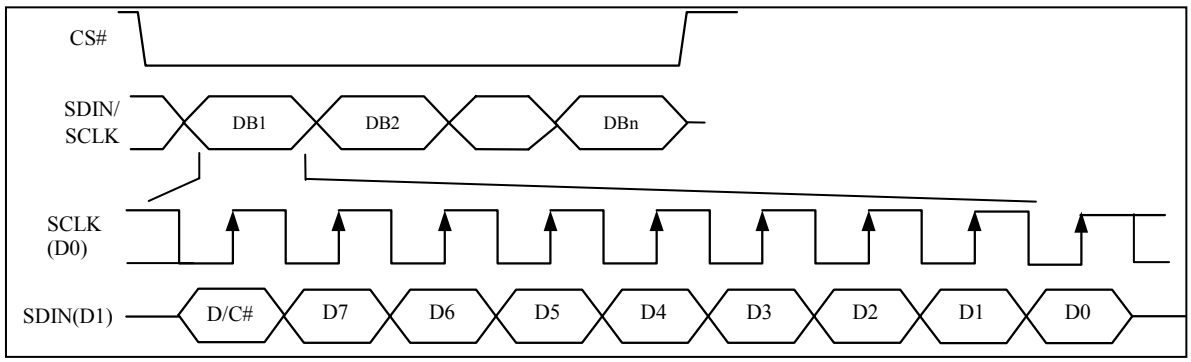
Under serial mode, only write operations are allowed.

Table 8-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.1.5 MCU I^2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1309 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1309. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

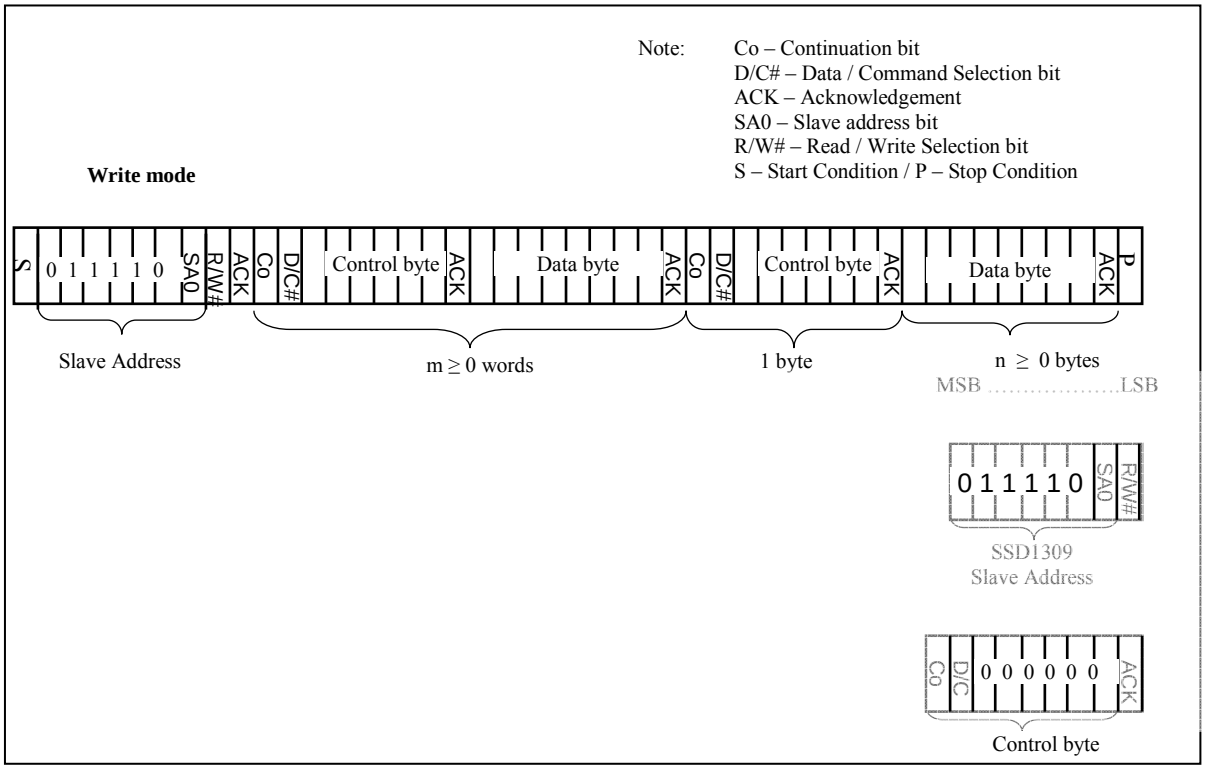
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I²C-bus in chronological order.

Figure 8-7 : I²C-bus data format



8.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1309, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

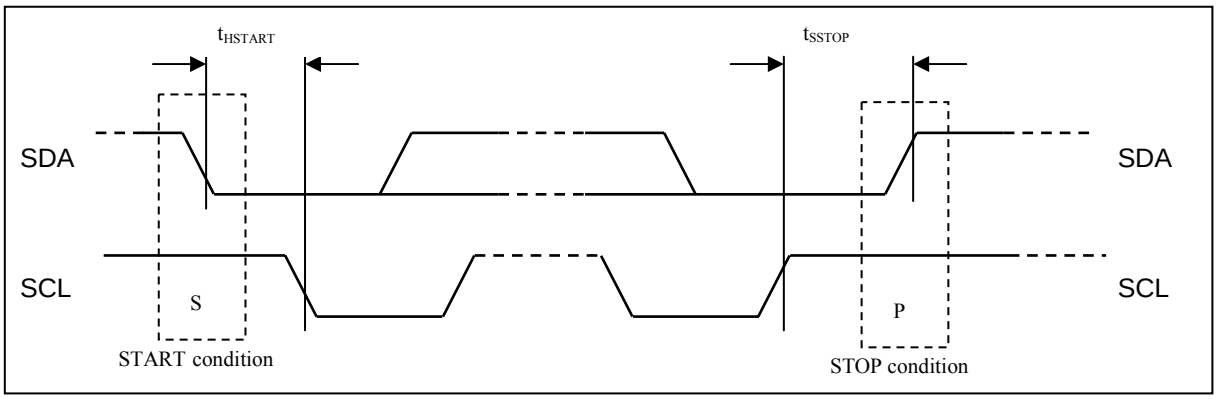
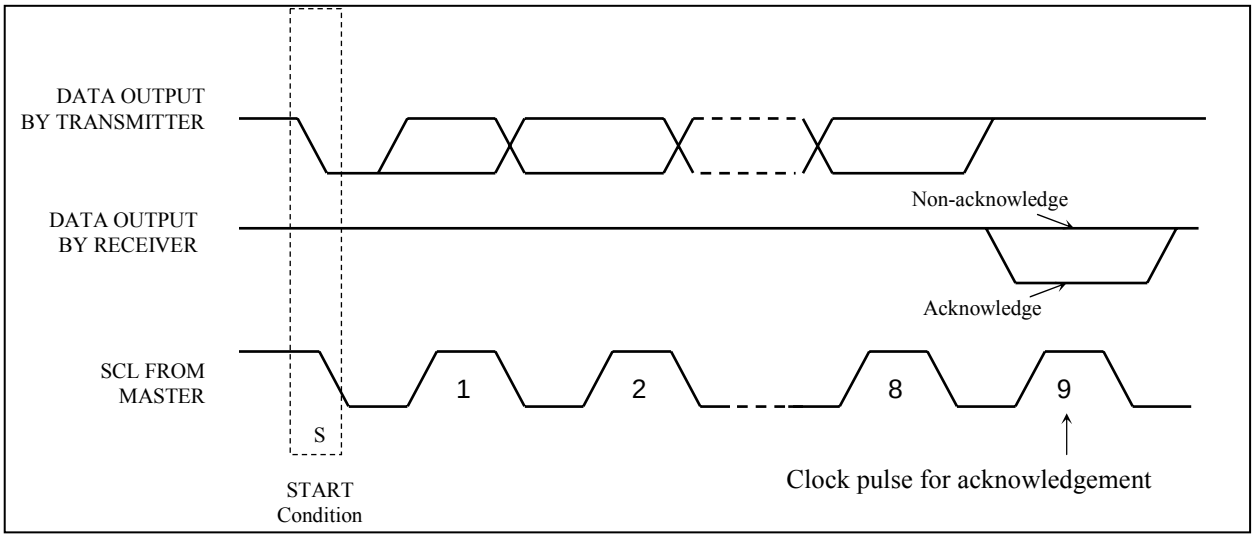


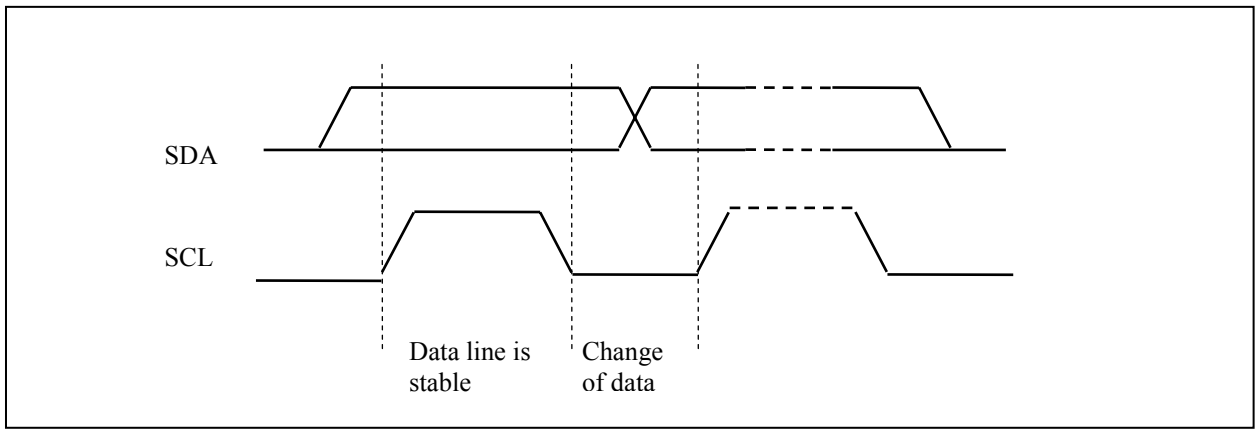
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-10 : Definition of the data transfer condition



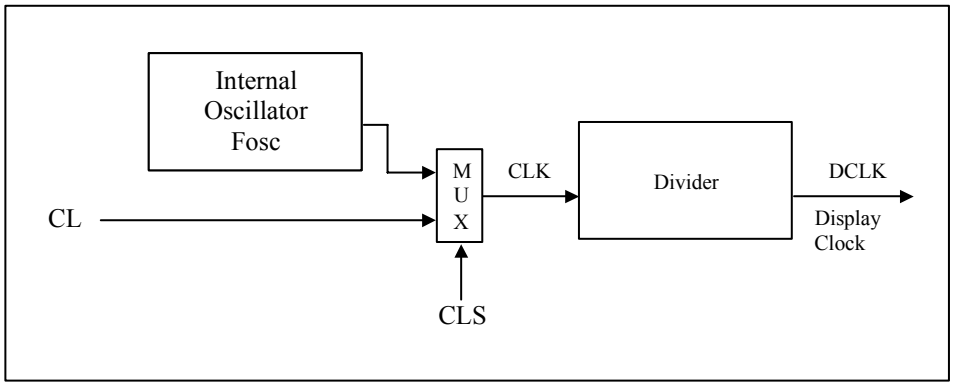
8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 2 + 2 + 65 = 69 at power on reset (that is K_o is a constant that equals to 65)
  (Please refer to Section 8.5 "Segment Drivers / Common Drivers" for the details of the "Phase")
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

8.4 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

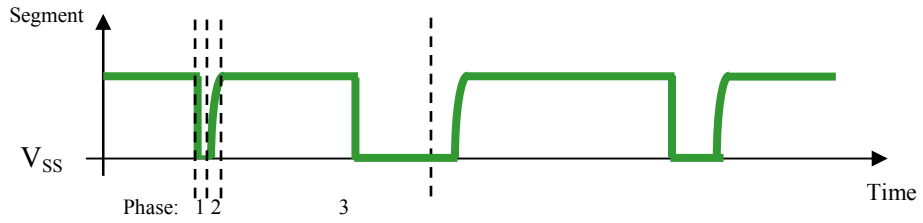
8.5 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 320uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 8-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 65, after finishing 65 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

8.6 Graphic Display Data RAM (GDDRAM)

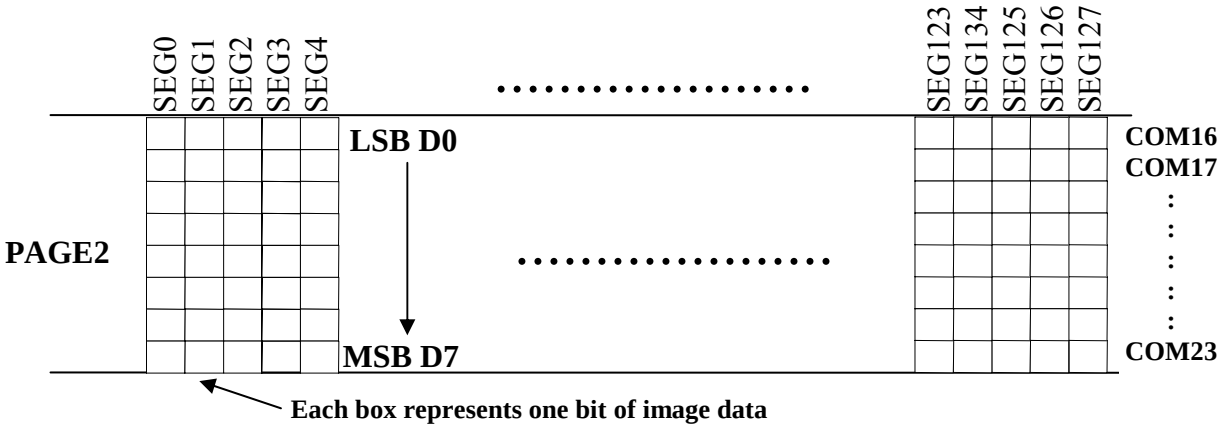
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1309

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.7 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

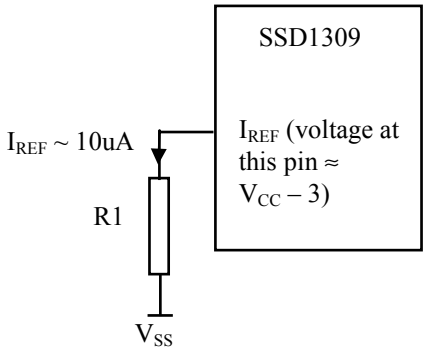
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = (Contrast+1) /8 x I_{REF}

  in which the contrast (0~255) is set by Set Contrast command 81h

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 8-15. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 320uA at maximum contrast 255.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 3) / 10uA
= 900kΩ